Analog Performance of Screen Grid Field Effect Transistor (SGrFET)

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A novel field effect transistor, Screen-Grid FET (SGrFET) designed with two rows of embedded MOS gate cylinders in the channel, has been proposed. This configuration allows full 3-D gate control of the current flow tolerating downscaling with limited short channel effects. Promising DC and switching characteristics of the structure have been previously presented. Here SGrFET's analog performance using 3-D TCAD Taurus^{TM} simulations are investigated. The hydrodynamic model in addition to the standard drift-diffusion model is used, taking surface scattering into account.

In particular, we study the influence of geometrical structure of the device on its characteristics, and its performance in comparison with finFET. AC small-signal simulation is carried out to obtain the relevant y-parameters as a function of frequencies and bias voltages. The high frequency parameters such as small-signal current gain (H21), and Mason unilateral power gain (U) can be derived, which yield the corresponding cut-off frequencies (f_T) and the maximum frequency of oscillation (f_{max}). However, since the device simulation is carried out ignoring any contact resistance and series resistance, these values are slightly over-estimated; especially f_{max} which values will not be presented here. Important parameters for analog circuit design such as transconductance (g_m), transconductance efficiency (g_m/I_{DS}), output resistance (r_o) and intrinsic gain (g_m/g_d) will also be of interest. Constant current is chosen as a comparison parameter since analog circuits are normally biased with fixed drain currents at saturation. All devices are n-type with lowly doped channel at $1X10^{14}cm^{-3}$ and source and drain doped at $1X10^{20}cm^{-3}$, channel width of 30nm and SOI active layer of 40nm.

Figure 1: Variation of g_m/I_{ds} and f_T for SGrFET with S-D distances of 60nm and 80nm.

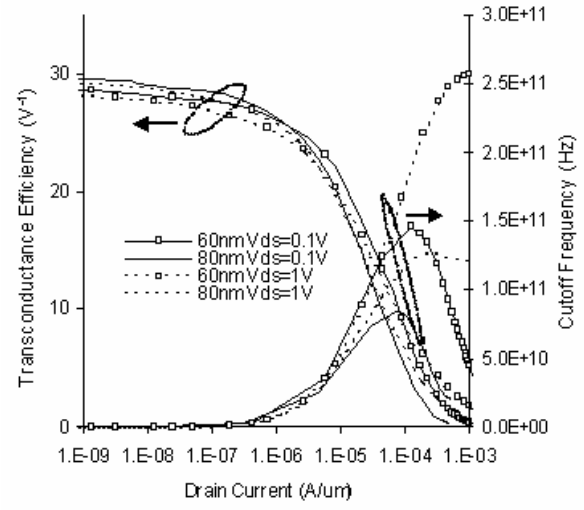

Figure 2: Extrapolated H_{21} and U at -20dB/dec for extraction of f_T and f_{max} at V_{DS}=1.0V and V_{GS}-V_T=0.2V for SGrFET and finFET with S-D distance of 60nm.

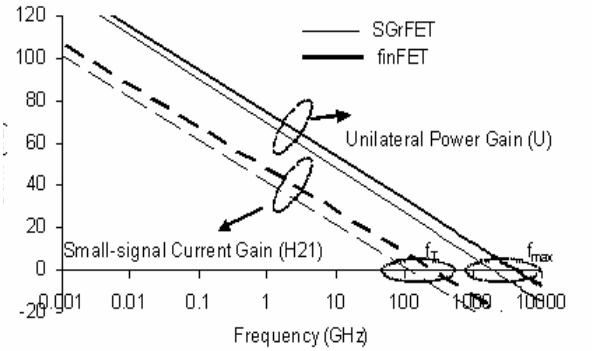

Table 1: Analog performance parameters extracted from small-signal simulation for SGrFET and finFET with S-D distance 80nm (V_{DS}=1.0V and I_{DS}=100µA/µm)

	g_m (µS/µm)	g_m/I_{DS} @ weak inversion (V^{-1})	r_o (kΩ.µm)	g_m/g_d	f_T (GHz)
SGrFET	650	29.4	25.0	16.3	118
finFET	960	26.5	14.0	13.4	210

Results show that SGrFET offers excellent analog performance, with higher transconductance efficiency and output resistance due to improved short channel behaviour. SGrFET also gives comparable RF performance in terms of cut-off frequency and intrinsic gain as the finFET, at similar dimension without any structure optimisations, giving a good trade-off between frequency response characteristic and low power performance.